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system-on-chip designs,  
critical to designers  
using 90-nanometer and  
below technology. The  
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About this book. "Tools  
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power methodology  
with a practical, step-by-  
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Kirtesh Tiwari...

Leveraging years of collective industry best practices, the

Verification

Methodology Manual

for Low Power (VMM-

LP) introduces a new

verification

methodology for low

power and provides a

blueprint for successful

verification of low

power designs. It

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describes the common causes of low power design failures, the impact of low power on the specification of power intent, the implementation of test plans, the setup of testbenches and the metrics of verification using assertions and coverage.

Verification

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step approach."

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A logical next step for the collaboration was to tackle a low-power design methodology, and after 10 years of collaboration, a team of technologists from ARM and Synopsys has produced the Low Power...

Low Power  
Methodology Manual:  
For System-On-Chip  
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Design ...odology

Low Power  
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Design (Integrated  
Circuits and Systems):  
David Flynn, Robert  
Aitken, Alan Gibbons,  
Kaijian Shi, Michael  
Keating:  
9780387718187:  
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with a practical, step-by-step approach.” Richard Goering, Software Editor, EE Times

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Methodology for SoC  
Designers John Biggs,  
ARM Ltd. and P1801  
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IEEE 1801-2013 ...

Low-power Design with  
the New IEEE

1801-2013 Standard

An integral piece of a  
functional verification  
plan, Cadence's power-  
aware verification

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Methodology can help  
verify power  
optimization without  
impacting design intent,  
minimizing late-cycle  
errors and debugging  
cycles. After all,  
simulating without  
power intent is like  
simulation with some  
RTL code black boxed.

Power-Aware  
Verification

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## Methodology

Summary of Contents  
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Page 1 CADENCE Low-

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KIT Meeting the power  
consumption and

density requirements of  
modern electronic

devices means engineers  
must consider power at

all stages of the design

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process—from architecture through implementation.

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